**LESSON PLAN**

**Name of the Faculty: Pency**

Discipline: Computer Engineering

Department: Computer Engineering

Semester: 3rd

Subject: Digital Electronics

Lesson Plan Duration: 15 weeks

**\*\*Work load (Lecture / Practical) per week(in hours): Lectures-03, Practicals -03**

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|  **Week** | Theory | Practical |
| Lect Day | Topic (including Assignment and Test) | Pract Day |  Topic |
| 1st | 1st | **1. Introduction**a) Distinction between analog and digital signal. | 1st | Verification and interpretation of truth tables for AND, OR, NOT gates |
| 2nd | b) Applications and advantages of digital signals. | 2nd | Verification and interpretation of truthtables for AND, OR, NOT gates |
| 3rd | **2. Number System**a) Binary, octal and hexadecimal number system: Conversion from decimal to binary | 3rd | Verification and interpretation of truth tables for AND, OR, NOT gates |
| 2nd | 1st | Conversion from hexadecimal to binary | 1st | Verification and interpretation of truth tables for NAND, NOR gates |
| 2nd | Conversion from binary to decimal | 2nd | Verification and interpretation of truthtables for NAND, NOR gates |
| 3rd | Conversion from binary to hexadecimal | 3rd | Verification and interpretation of truth tables for Exclusive OR (EXOR) gate |
| 3rd | 1st | b) Binary addition and subtraction including binary points. 1’s and 2’s complement method of addition/subtraction. | 1st | Verification and interpretation of truth tables for Exclusive OR (EXOR) gate |
| 2nd | **3. Codes and Parity**a) Concept of code, weighted and non-weighted codes | 2nd | Verification and interpretation of truth tables for Exclusive OR (EXOR) gate |
| 3rd | Examples of 8421, BCD,Excess-3 and Gray code. | 3rd | Verification and interpretation of truthtables forExclusive NOR(EXNOR) gate |
| 4th | 1st | b) Concept of parity, single and double parity, Error detection | 1st | Verification and interpretation of truth tables forExclusive NOR(EXNOR) gate |
| 2nd | **4. Logic Gates and Families**a) Concept of negative and positive logic NOT, AND, OR, NAND, NOR, EXOR Gates | b) Definition, symbols and truth tables of | 2nd | Verification and interpretation of truth tables forExclusive NOR(EXNOR) gate |
| 3rd | NAND & NOR as universal gates. logic families | (c) Introduction to TTL and CMOS | 3rd | Realisation of logic functions with the help of NAND gate |
| 5th | 1st | **5. Logic Simplification**a) Postulates of Boolean algebra, De Morgan’s Theorems. | 1st | Realisation of logic functions with the helpof NAND gate |
| 2nd | Implementation of Boolean (logic) equation with gates | 2nd | Realisation of logic functions with the help of NOR gate |
| 3rd | Implementation of Boolean (logic) equation with gates | 3rd | Realisation of logic functions with the help of NOR gate |
| 6th | 1st | Karnaugh map (2 variables) and simple application in developing combinational logic circuits | 1st | To design a half adder using XOR gateand verification of its operation |
| 2nd | Karnaugh map (3 variables) and simple application in developing combinational logic circuits | 2nd | To design a half adder using XOR gate and verification of its operation |
| 3rd | Karnaugh map (4 variables) and simple application in developing combinational logic circuits | 3rd | To design a half adder using NAND gate and verification of its operation |
| 7th | 1st | Karnaugh map (4 variables) and simple application in developing combinational logic circuits | 1st | To design a half adder using NAND gate and verification of its operation |
| 2nd | **6. Arithmetic circuits**Half adder circuit, design and implementation. | 2nd | Construction of a full adder circuit using XOR gate and verify its operation |
| 3rd | Full adder circuit, design and implementation. | 3rd | Construction of a full adder circuit using NAND gate and verify its operation |
| 8th | 1st | 4 bit adder circuit | 1st | Construction of a full adder circuit using NAND gate and verify its operation |
| 2nd | **7. Decoders, Multiplexeres, De Multiplexeres and Encoder**a) Four bit decoder circuits for 7 segment display and decoder/driver ICs. | 2nd | Verification of truth table for positive edge triggered IC flip-flops of D latch |
| 3rd | b) Basic functions and block diagram of MUX with different Ics | 3rd | Verification of truth table for positive edge triggered IC of D flip-flop |
| 9th | 1st | b) Basic functions and block diagram of DEMUX with different Ics | 1st | Verification of truth table for positive edgetriggered IC of JK flip-flops. |
| 2nd | c) Basic functions and block diagram of Encoder | 2nd | Verification of truth table for Negativeedge triggered IC flip-flops of D latch |
| 3rd | **8. Latches and flip flops**a) Concept and types of latch with their working and applications | 3rd | Verification of truth table for negative edge triggered IC of D flip-flop |
| 10th | 1st | b) Operation using waveforms and truth tables of RS & T flip flops. | 1st | Verification of truth table for negative edge triggered IC of JK flip-flops. |
| 2nd | Operation using waveforms and truth tables of D & Master/Slave flip flops. | 2nd | Verification of truth table for level triggered IC flip-flops of D latch |
| 3rd | Operation using waveforms and truth tables of JK flip flops. c) Differencebetween a latch and a flip flop | 3rd | Verification of truth table for level triggered IC of D flip-flop |
| 11th | 1st | **9. Counters**a) Introduction to Asynchronous and Synchronous counters | 1st | Verification of truth table for leveltriggered IC of JK flip-flops. |
|  | 2nd | b) Binary counters | 2nd | Verification of truth table for encoder Ics |
| 3rd | c) Divide by N ripple counters, Decade counter | 3rd | Verification of truth table for decoder ICs |
| 12th | 1st | Ring counter | 1st | Verification of truth table for Mux |
| 2nd | **10. Shift Register**Introduction and basic concepts including shift left and shift right. | 2nd | Verification of truth table for DeMux |
| 3rd | a) Serial in parallel out, serial in serial out | 3rd | To design a 4 bit SISO shift registers using JK/D flip flops and verification of their operation. |
| 13th | 1st | Parallel in serial out, parallel in parallel out. | 1st | To design a 4 bit SIPO shift registersusing JK/D flip flops and verification of their operation. |
| 2nd | b) Universal shift register | 2nd | To design a 4 bit PISO shift registersusing JK/D flip flops and verification of their operation. |
| 3rd | **11. A/D and D/A Converters**Working principle of A/D and D/A converters | 3rd | To design a 4 bit PIPO shift registers using JK/D flip flops and verification oftheir operation. |
| 14th | 1st | Brief idea about different techniques of A/D conversion Study of* Stair step Ramp A/D converter
 | 1st | To design a 4 bit ring counter and verify its operation. |
| 2nd | * Dual Slope A/D converter
* Successive Approximation A/D Converter
 | 2nd | To design a 4 bit ring counter and verifyits operation. |
| 3rd | Detail study of :* Binary Weighted D/A converter
* R/2R ladder D/A converter
 | 3rd | To design a 4 bit ring counter and verify its operation. |
| 15th | 1st | * R/2R ladder D/A converter Applications of A/D and D/A converter.
 | 1st | Use of Asynchronous Counter ICs (7490 or 7493) |
| 2nd | **12. Semiconductor Memories**Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM) | 2nd | Use of Asynchronous Counter ICs (7490 or 7493) |
| 3rd | Static and dynamic RAM, Introduction to 74181 ALU IC | 3rd | Use of Asynchronous Counter ICs (7490 or 7493) |